

REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 11-17 are presently active in this case.

In the outstanding Office Action, Claims 11-17 were finally rejected under 35 U.S.C. §102(b) as being anticipated by Quigley et al (U.S. Pat. No. 5,708,288).

Applicants acknowledge with appreciation the telephone interview between the Examiner and Applicants' representative on May 27, 2003.

Briefly recapitulating, Claim 11 is directed to a device for protection of an electronic component against electrostatic discharges, comprising a plurality of Zener diodes formed in a semiconducting layer of a substrate, the semiconducting layer covering an insulating layer and having two regions of heavy doped opposite conductivity types with at least one of the two regions extending to the insulating layer. The protection device also includes a contact pin connected to the electronic component and connected through the Zener diodes to ground in order to divert an electrostatic discharge and thereby protect the electronic component. By embedding a plurality of Zener diodes in a substrate, a sufficient number of Zeners may be compactly arranged in series to resist power supply voltages without inducing excessive leakage.¹

Quigley discloses a thin film silicon on insulator circuit with four zener diodes 26, 27, 28, 29 and a low voltage triggering apparatus (LVTA) 36, where the LVTA 36 is a zener diode formed within the boundaries of surface silicon controlled rectifier 30 and comprises P+ doped zener region 242, field oxide regions 145, N- doped zener region 244, and N+

¹ Specification, page 14, lines 1-5 and lines 14-18; Figures 4-6.

doped zener region 244.² As discussed during the telephone interview of May 27, 2003, Quigley does not disclose “a *plurality* of Zener diodes formed in a semiconducting layer of a substrate” as recited in Applicants’ Claim 11. LVTA 36 is a *single* Zener diode formed within the boundaries of surface silicon controlled rectifier 30.

Also, contrary to the statement in the pending Official Action,³ Zener diodes 26, 27, 28, 29 are not formed in the same semiconducting layer of substrate as LVTA 36 but instead are separate diodes connected to LVTA 36 via various other devices and connections. Instead, Applicants submit that Zener diodes 26, 27, 28, 29 of Quigley are comparable to Applicants’ diodes 26 as they are “classical inverse polarized diodes [located] at several locations in the circuit in order to [complete the protection device] and increase the efficiency of the protection.” Therefore, Zener diodes 26, 27, 28, 29 and LVTA 36 do not comprise a plurality of Zener diodes formed in a semiconducting layer of a substrate.

Since the cited reference does not disclose or suggest all the elements of independent Claim 11, Applicants submit the inventions defined by Claim 11, and all claims depending therefrom, are not anticipated and respectfully request the rejection be withdrawn.⁴

² Quigley, column 3, lines 2-11; column 4, lines 9-22; Figures 1-3.

³ Official Action, page 2.

⁴ MPEP § 2142 “...the prior art reference (or references when combined) must teach or suggest **all** the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).”

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Accordingly, in view of the present amendment and ~~in light of the previous~~ discussion, it is respectfully submitted that the application is believed in condition for allowance and early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Registration No. 28,870
Attorney of Record
Michael E. Monaco
Registration No. 52,041



22850

Tel.: (703) 413-3000
Fax: (703) 413-2220
EHK/MEM/kkn

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